Notice of Allowability	Application No.	Applicant(s)	
	10/057,626	MORONEY ET AL.	
	Examiner	Art Unit	
	Ranodhi Serrao	2141	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *13 September 2007*.

2. ☒ The allowed claim(s) is/are *1 and 5-14*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

WILLIAM VAUGHN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER

Interview Summary

1. A proposed amendment was submitted for applicant's consideration. Examiner suggested the Applicant to amend claims as shown in the Examiner's Amendment below in order to place the application in condition for allowance.

Examiner's Amendment

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. Authorization for this examiner's amendment was given in a telephone interview with the Applicant's Representative, Mr. Glenn M. Kubota (Reg. No. 44,197), on 27 September 2007.

Amendment to the Claims

Please amend claims 6 and 11 and cancel claims 15 and 16 as below:

Claim 6. (Currently Amended) The system of claim [[4]] 1, further comprising a translation-memory accessible to each of the microsequencers of said first and second microsequencer systems, said translation-memory having

a translation-memory address, and

a translation-memory element corresponding to said translation-memory address, said translation-memory element including data for musing an instruction-memory pointer to jump to a selected instruction word.

Claim 11. (Currently Amended) The system of claim [[4]] 1, further comprising a translation- memory having:

a translation-memory address;

a first translation-memory element corresponding to said translation-memory address, said first translation-memory element including data for causing an instruction-memory pointer to jump to a first instruction word;

a second translation-memory element corresponding to said translation-memory address, said second translation-memory element including data for causing said instruction-memory pointer to jump to a second instruction word; and

a selector for selecting said first translation-memory element.

Claim 15. (Canceled)

Claim 16. (Canceled)

Allowable Subject Matter

4. Claims 1 and 5-14 are allowed. The following is an examiner's statement of reasons for allowance: In interpreting the claims, in light of the specification and the authorized Examiner's Answer on 27 September 2007, the Examiner finds the claimed invention to be patentably distinct from the prior art of record.

5. **Yao et al. (2003/0084219)** teaches a system, apparatus and method for an efficiently performing address lookups and switching for computer networks is disclosed. The present disclosure provides for address translation between network devices utilizing different protocols. The system, apparatus and method described herein provide for address translation for encapsulated communications to enable mixed protocol communications using a network switch fabric system **(Yao, abstract, Figure 1, and corresponding text).**

6. Satou et al. (5,717,946) teaches a data processor having a string operation instruction and a bit map operation instruction, and comprises a bus interface unit 157 which inputs/outputs data by the burst transfer function, and an integer operation unit 155 building-in a main ALU and a sub-ALU, wherein data is repeatedly transferred to/from an external memory via a data bus 102 in unit greater than a width of the data bus 102. Further, is can be accessed in a high speed by the block transfer in the burst mode to efficiently execute the above instructions, therefore the data string and bit map data can be executed quickly even when a low-cost slow memory system is connected thereto **(Satou, abstract, Figure 16, and corresponding text).**

7. Byers et al. (5,809,543) teaches an outboard file cache extended processing complex for use with a host data processing system for providing closely coupled file

caching capability is described. Data movers at the host provide the hardware interface to the outboard file cache, provide the formatting of file data and commands, and control the reading and writing of data from the extended processing complex. Host interface adapters receive file access commands sent from the data movers and provide cache access control. Directly coupled fiber optic links couple each of the data movers to the associated one of the host interface adapters and from the nonvolatile memory. A nonvolatile memory to store redundant copies of the cached file data is described. A system interface including bidirectional bus structures and index processors that control the routing of data signals, provides control of storage and retrieval of file cache data derived from host interface adapters and from the nonvolatile memory. Multiple power domains are described together with independent clock distribution within each power domain. The independent clock distribution sources are synchronized with each other. A system for fault tolerant redundant storage of file cache data redundantly in at least two portions of the nonvolatile file cache storage is described **(Byers, abstract, Figure 29, and corresponding text).**

8. However, the prior art of record fail to teach or suggest individually or in combination a system for enabling communication between a first network having a first network protocol and a second network having a second network protocol, the second network being a storage area network, said system comprising: a first data port for receiving first input data and first state information from said first network, said first input data being expressed in said first network protocol; a second data port for receiving second input data and second state information from said second network, said second

input data being expressed in said second network protocol; a first microsequencer system configured to translate said second input data into corresponding data expressed in said first network protocol on the basis of said first state information, the first microsequencer system including one or more microsequencers configured to cooperate in translating said second input data into corresponding data expressed in said first network protocol; a second microsequencer system configured to translate said first input data into corresponding data expressed in said second network protocol on the basis of said second state information, the second microsequencer system including one or more microsequencers configured to cooperate in translating said first input data into corresponding data expressed in said second network protocol; and an instruction memory accessible to each of the microsequencers of the first and second microsequencer systems, said instruction memory having a plurality of instruction words, each of said instruction words forming a Very Long Instruction Word (VLIW) having a plurality of instruction fields executable in parallel by different functional units of each of the microsequencers to enable the microsequencers to execute a plurality of instructions in a single instruction cycle, **the instruction memory being loadable via a processor interface to make the microsequencers programmable to accommodate different first and second network protocols.**

9. These limitations, in conjunction with the other limitations in the independent claim, are not specifically disclosed or remotely suggested in the prior art of record. Therefore, claims 1 and 5-14 are allowed.

10. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ranodhi Serrao whose telephone number is (571) 272-7967. The examiner can normally be reached on 8:00-4:30pm, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rupal Dharia can be reached on (571) 272-3880. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RNS

R.N.S.

9/28/2007

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